Abstracts

Implementation of a real-time frequency-selective RF channel simulator using a hybrid DSP-FPGA architecture

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A low cost frequency-selective RF channel simulator architecture is explored in this paper. The technique of quadrature amplitude modulation (QAM) by independent low-pass filtered white Gaussian noise sources forms a rational function approximation (RFA) to the desired Doppler spectrum for flat Rayleigh fading. To simulate frequency-selective fading, this QAM/RFA architecture may be extended by combining delayed outputs from multiple flat fading generators. In this paper, the noise shaping filter considered is in the form of an infinite-impulse-response digital filter followed by an interpolator (upsampler) using linear interpolation. The performance requirements are those in the standard channel simulator section of TIA IS-55-A. The system is implemented almost entirely in the digital domain by use of IF sampling, with the signal processing performed in a high-end floating-point digital signal processor and a field-programmable gate array. The theoretical performance of the simulator is studied with respect to the TIA standard, and limitations of the hardware prototype are identified. A system capable of simulating 12 delay taps, with a processing bandwidth of 5 MHz, can be built at about one-tenth the cost of commercially available channel simulators of comparable performance.

❑ Return to main document.